Amendments to the Specification:

Rewrite paragraph **[0023]** at page 11 as follows:

In the step-by-step mode, the second processor fetches a supported instruction from memory 206 through memory bus 222, and loads the instruction in the decode logic 210 of the first processor 202. In at least some embodiments, the switch 230 closes when the first processor 202 transitions to the step-by-step mode so that the decode ~~control~~ logic 210 ~~218~~ is connected to port 214 and may be accessed by the second processor 204. The switch 230 may comprise any electrical apparatus for controlling the coupling of port 214 to decode logic 210. The second processor 204 may load supported instructions to the decode logic 210 of the first processor 202 using a memory mapped instruction buffer, co-processor instruction, or other instruction, wherein the supported instructions are sent from the second processor 204 via the inter-processor bus 220, port 214, and switch 230 to the decode logic 210 of first processor 204 for decoding and subsequent execution in the first processor 202.